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Title: HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES
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HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES

Cross Reference To Related Applications

This application is related to the following co-pending, commonly assigned U.S. patent applications: "Programmable Logic Arrays with Transistors with Vertical Gates," attorney docket no. 303.683US1, serial number _____, and "Programmable Memory Decode Circuits with Vertical Gates," attorney docket no. 303.692US1, serial number _____, which are filed on even date herewith and each of which disclosure is herein incorporated by reference.

Technical Field of the Invention

This invention relates generally to integrated circuits and in particular to horizontal memory devices with vertical gates.

Background of the Invention

One difficulty with EEPROM, EAPROM, and flash memory devices is the adverse capacitance ratio between the control gate and the floating gate. That is, the capacitance between the control gate to floating gate (CCG) is about the same as the floating gate to substrate capacitance (CFG). Figure 1A is an illustration of a horizontal EEPROM, EAPROM, or flash memory device formed according to the teachings of the prior art. As shown in Figure 1A, conventional horizontal floating gate transistor structures include a source region 110 and a drain region 112 separated by a channel region 106 in a horizontal substrate 100. A floating gate 104 is separated by a thin tunnel gate oxide 105 shown with a thickness (t1). A control gate 102 is separated from the floating gate 104 by an intergate dielectric 103 shown with a thickness (t2). Such conventional devices must by necessity have a control gate 102 and a floating gate 104 which are about the same size in width.

Figure 1B is an illustration of a vertical EEPROM, EAPROM, or flash memory device formed according to the disclosure in a co-pending, commonly assigned application by W. Noble and L. Forbes, entitled "Field programmable logic array with vertical transistors," serial no. 09/032617, filed February 27, 1998. Figure 1B illustrates that vertical floating gate transistor structures have a stacked source region 110 and drain region 112 separated by a vertical channel region 106. The vertical floating gate transistor shown in Figure 1B further includes a vertical floating gate 104 separated by a thin tunnel gate oxide 105 from the channel region 106. A vertical control gate 102 is separated from the floating gate 104 by an intergate dielectric 103. As shown in Figure 1B, the vertical control gate 102 and the vertical floating gate 104 are likewise about the same size in width relative to the channel region 106.

Conventionally, the insulator, or intergate dielectric, 103 between the control gate 102 and the floating gate 104 is thicker (t2) than the gate oxide 105 (t1) to avoid tunnel current between the gates. The insulator, or intergate dielectric, 103 is also generally made of a higher dielectric constant insulator 103, such as silicon nitride or silicon oxynitride. This greater insulator thickness (t2) tends to reduce capacitance. The higher dielectric constant insulator 103, on the other hand, increases capacitance. As shown in Figure 1C, the net result is that the capacitance between the control gate and the floating gate (CCG) is about the same as the gate capacitance of the thinner gate tunneling oxide 105 between the floating gate and the substrate (CFG). This undesirably results in large control gate voltages being required for tunneling, since the floating gate potential will be only about one half that applied to the control gate.

As design rules and feature size (F) in floating gate transistors continue to shrink, the available chip surface space in which to fabricate the floating gate also is reduced. In order to achieve a higher capacitance between the control gate and floating gate (CCG) some devices have used even higher dielectric constant insulators between the control gate and floating gate. Unfortunately, using such

higher dielectric constant insulators involves added costs and complexity to the fabrication process.

Therefore, there is a need in the art to provide memory devices which can operate with lower control gate voltages and which do not increase the costs or complexity of the fabrication process. Further such devices should desirably be able to scale with shrinking design rules and feature sizes in order to provide even higher density integrated circuits.

Summary of the Invention

The above mentioned problems with memory devices and other problems are addressed by the present invention and will be understood by reading and studying the following specification. Structures and methods for memory devices are provided which can operate with lower applied control gate voltages than conventional floating gate transistor memory devices, and which do not increase the costs or complexity of the device fabrication process. These systems and methods are fully scalable with shrinking design rules and feature sizes in order to provide even higher density integrated circuits. The total capacitance of these memory devices is about the same as that for the prior art of comparable source and drain spacings. However, according to the teachings of the present invention, the floating gate capacitance is much smaller than the control gate capacitance such that the majority of any voltage applied to the control gate will appear across the floating gate thin tunnel oxide. Thus, the devices of the present invention can be programmed by tunneling of electrons to and from the silicon substrate at lower control gate voltages than is possible in the prior art.

In one embodiment of the present invention, a novel memory cell is provided. The memory cell includes a source region and a drain region separated by a channel region in a horizontal substrate. A first vertical gate is separated from a first portion of the channel region by a first oxide thickness. A second vertical gate is separated from a second portion of the channel region by a second oxide

thickness. According to one embodiment the memory cell includes a flash memory cell. In another embodiment, the memory cell includes an electronically erasable and programmable read only memory (EEPROM) cell. In another embodiment, the memory cell includes an electronically alterable and programmable read only memory (EAPROM) cell. In one embodiment of the present invention, the first vertical gate and the second vertical gate have a horizontal width of approximately 100 nanometers (nm). Also, in one embodiment the first oxide thickness is approximately 60 Angstroms (Å) and the second oxide thickness is approximately 100 Angstroms (Å).

Another embodiment of the present invention includes a method for forming a novel memory cell. The method includes forming a source region and a drain region separated by a channel region in a horizontal substrate. The method includes forming a first vertical gate above a first portion of the channel region and separated from the channel region by a first oxide thickness. The method further includes forming a second vertical gate above a second portion of the channel region and separated from the channel region by a second oxide thickness. Forming the second vertical gate includes forming the second vertical gate parallel to and opposing the first vertical gate.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1A is an illustration of a horizontal EEPROM, EAPROM, or flash memory device formed according to the teachings of the prior art.

Figure 1B is an illustration of a vertical EEPROM, EAPROM, or flash memory device formed according to the teachings of the existing art.

Figure 1C is a schematic diagram illustrating the generally equivalent capacitances of the control gate (CCG) and the floating gate (CFG) according to the existing art.

Figure 2A is a block diagram of an embodiment for a novel memory cell, transistor, or floating gate transistor formed according to the teachings of the present invention.

Figure 2B is a schematic diagram illustrating the respective capacitances between the between respective components of the novel memory cell shown in Figure 2A.

Figure 2C is a simplified schematic diagram representing the same capacitance relationship shown in Figure 2B.

Figure 3A is a block diagram of another, asymmetrical embodiment for a novel memory cell, transistor, or floating gate transistor formed according to the teachings of the present invention.

Figure 3B is a schematic diagram illustrating the respective capacitances between the between respective components of the novel memory cell shown in Figure 3A.

Figure 3C is a simplified schematic diagram representing the same capacitance relationship shown in Figure 3B.

Figures 4A-4I illustrate embodiments of the methods for forming the novel memory cell, transistor or floating gate transistor according to the teachings of the present invention.

Figures 5A-5E are block diagrams illustrating embodiments of the methods for operating the novel memory cells of the present invention.

Figure 6 is a schematic drawing illustrating one circuit diagram embodiment and application for the novel memory cells of the present invention.

Figure 7 illustrates a block diagram of an embodiment of an electronic system including a novel memory cell formed according to the teachings of the present invention.

Figure 8 illustrates an embodiment of a memory array including a novel memory cell formed according to the teachings of the present invention, as can be included in a memory device, e.g. on a memory chip/die.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The terms wafer and substrate used in the following description include any base semiconductor structure. Both are to be understood as including bulk silicon material, silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure and layer formed above, and the terms wafer or substrate include the underlying layers containing such regions/junctions and layers that may have been

formed above. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Figure 2A is a block diagram of an embodiment for a novel memory cell, transistor, or floating gate transistor 201 formed according to the teachings of the present invention. As shown in Figure 2A, the memory cell 201 includes a source region 210 and a drain region 212 separated by a channel region 206 in a horizontal substrate 200. According to the teachings of the embodiment shown in Figure 2A, the memory cell 201 includes a first vertical gate 202 located above a first portion, or first region, 207-1, of the channel region 206. In one embodiment, the first vertical gate 202 includes or serves as a floating gate 202 for the memory cell 201. In an alternative embodiment, the first vertical gate 202 includes or serves as a control gate 202 for memory cell 201. The first vertical gate is separated from the channel region 206 by a first thickness insulator material, or first oxide thickness (t1). A second vertical gate 204A is located above a second portion, or second region, 207-2 of the channel region 206. The second vertical gate 204A is separated from the channel region 206 by a second thickness insulator material, or second oxide thickness (t2). The memory cell 201 embodiment shown in Figure 2A further includes a third vertical gate 204C located above a third portion, or third region, 207-3 of the channel region 206. The third vertical gate is separated from the channel region 206 by the second thickness insulator material, or second oxide thickness (t2). In one embodiment of the present invention, the first oxide thickness (t1) is approximately 60 Angstroms (Å) and the second oxide thickness (t2) is approximately 100 Angstroms (Å). According to the teachings of the present invention, the first thickness insulator material (t1) and the second thickness insulator material (t2) are formed of silicon dioxide (SiO_2).

As shown in the embodiment of Figure 2A, the second and the third vertical gates, 204A and 204C respectively, are parallel to and on opposing sides of the first vertical gate 202 forming a symmetrical structure. The memory cell 201 embodiment of Figure 2A further includes a horizontal gate member 204B which couples the second 204A and the third 204C vertical gates. The horizontal gate member 204B is located above the first vertical gate 202 and separated therefrom by an intergate dielectric 203. In the embodiment shown in Figure 2A, the second and the third portion, 207-2 and 207-3 respectively, of the channel region 206 are adjacent to the source region 210 and the drain region 212 respectively.

According to one embodiment of the present invention, the first vertical gate 202, the second vertical gate 204A, the horizontal gate member 204B, and the third vertical gate 204C include polysilicon gates which are separated from one another by the intergate dielectric 203. According to the teachings of the present invention, the intergate dielectric includes an intergate dielectric formed from silicon dioxide (SiO_2). In one embodiment, the intergate dielectric 203 between the first vertical gate 202, the second vertical gate 204A, the horizontal gate member 204B, and the third vertical gate 204C has a thickness approximately equal to the first oxide thickness (t1), or first thickness insulator material. In one embodiment of the present invention, the first vertical gate 202, the second vertical gate 204A, and the third vertical gate 204C each have a horizontal width of approximately 100 nanometers (nm).

As described above, in one embodiment, the first vertical gate 202 in memory cell 201 serves as a floating gate 202. In this embodiment, the second vertical gate 204A, the horizontal gate member 204B, and the third vertical gate 204C serve as control gates. In an alternative embodiment, the first vertical gate 202 in memory cell 201 serves as a control gate for the memory cell 201. In this embodiment, the second vertical gate 204A, the horizontal gate member 204B, and the third vertical gate 204C serve as floating gates. In one embodiment, the first

vertical gate 202, the second vertical gate 204A, and the third vertical gate 204C have a vertical height, respectively, of approximately 500 nanometers (nm).

Figure 2B is a schematic diagram illustrating the respective capacitances between the between the first vertical gate 202, the second vertical gate 204A, the horizontal gate member 204B, and the third vertical gate 204C, e.g. the control gate capacitance (CCG), as well as between these vertical gates and the channel region 206, e.g. the floating gate capacitance (CFG). Figure 2C is a simplified schematic diagram representing the same capacitance relationship. Thus, according to the teachings of the present invention, a greater percentage of a voltage applied to the control gate appears between the floating gate and the channel than between the control gate and the floating gate. This is true, since as shown in Figures 2B and 2C, the floating gate capacitance (CFG) of the present invention is much smaller than the control gate capacitance (CCG).

According to the teachings of the present invention, the total capacitance of these memory devices is about the same as that for the prior art of comparable source and drain spacings. However, according to the teachings of the present invention, the floating gate capacitance is much smaller than the control gate capacitance such that the majority of any voltage applied to the control gate will appear across the floating gate thin tunnel oxide. Thus, the devices of the present invention can be programmed by tunneling of electrons to and from the silicon substrate at lower control gate voltages than is possible in the prior art.

Figure 3A is a block diagram of another, asymmetrical embodiment for a novel memory cell, transistor, or floating gate transistor 301 formed according to the teachings of the present invention. As shown in Figure 3A, the memory cell 301 includes a source region 310 and a drain region 312 separated by a channel region 306 in a horizontal substrate 300. According to the teachings of the embodiment shown in Figure 3A, the memory cell 301 includes a first vertical gate 302 located above a first portion, or first region, 307-1, of the channel region 306. In one embodiment, the first vertical gate 302 includes or serves as a vertical floating gate

302 for the memory cell 301. In an alternative embodiment, the first vertical gate 302 includes or serves as a vertical control gate 302 for memory cell 301. The first vertical gate is separated from the channel region 306 by a first thickness insulator material, or first oxide thickness (t1). A second vertical gate 304A is located above a second portion, or second region, 307-2 of the channel region 306. The second vertical gate 304A is parallel to and opposes the first vertical gate 302 and is separated therefrom by an intergate dielectric 303. The second vertical gate 304A is separated from the channel region 306 by a second thickness insulator material, or second oxide thickness (t2). According to the teachings of the present invention, the first thickness insulator material (t1) and the second thickness insulator material (t2) are formed of silicon dioxide (SiO_2). In one embodiment, the first thickness insulator material (t1) is approximately 60 Angstroms (Å), and wherein the second thickness insulator material (t2) is approximately 100 Angstroms (Å).

According to one embodiment of the present invention, the second vertical gate 304A includes a horizontal gate member 304B which couples to the second vertical gate 304A and is separated from the first vertical gate by the intergate dielectric 303. As shown in Figure 3A, the horizontal member 304B is located above a portion of the first vertical gate 302. According to the teachings of the present invention, the intergate dielectric includes an intergate dielectric formed from silicon dioxide (SiO_2). In one embodiment, the intergate dielectric 303 between the first vertical gate 302, the second vertical gate 304A, and the horizontal gate member 304B has a thickness approximately equal to the first oxide thickness (t1), or first thickness insulator material. In one embodiment of the present invention, the first vertical gate 302 and the second vertical gate 304A each have a horizontal width of approximately 100 nanometers (nm). In one embodiment, the first vertical gate 302 and the second vertical gate 304A respectively each have a vertical height of approximately 500 nanometers (nm).

As shown in Figure 3A, the first vertical gate 302 which is separated from a first portion 307-1 of the channel region is separated from a first portion 307-1 of

the channel region 306 which includes a portion of the channel region 306 adjacent to the source region 310. The second vertical gate 304A which is separated from a second portion 307-2 of the channel region 306 is separated from a second portion 307-2 of the channel region which includes a portion of the channel region 306 adjacent to the drain region 312. As one of ordinary skill in the art will understand upon reading this disclosure, the relationship of the structure shown in Figure 3A to the source and drain regions, 310 and 312 respectively, can be reversed. As shown in Figure 3A, in one embodiment of the present invention, source and/or drain region extension, such as source extension 311, are included in memory cell 301. As will be understood by one of ordinary skill in the art upon reading this disclosure, the same can apply to the memory cell structure shown in Figure 2A.

Figure 3B is a schematic diagram illustrating the respective capacitances between the between the first vertical gate 302, the second vertical gate 304A, and the horizontal gate member 304B, e.g. the control gate capacitance (CCG), as well as between these vertical gates and the channel region 306, e.g. the floating gate capacitance (CFG). Figure 3C is a simplified schematic diagram representing the same capacitance relationship. Thus, according to the teachings of the present invention, a greater percentage of a voltage applied to the control gate appears between the floating gate and the channel than between the control gate and the floating gate. This is true, since as shown in Figures 3B and 3C, the floating gate capacitance (CFG) of the present invention is much smaller than the control gate capacitance (CCG). In other words, a capacitance between the vertical control gate 304A and the floating gate 302 (CCG) is greater than a capacitance between the floating gate 302 and the channel 306 (CFG).

Hence again, according to the teachings of the present invention, the total capacitance of these memory devices is about the same as that for the prior art of comparable source and drain spacings. However, according to the teachings of the present invention, the floating gate capacitance is much smaller than the control gate capacitance such that the majority of any voltage applied to the control gate will

appear across the floating gate thin tunnel oxide. Thus, the devices of the present invention can be programmed by tunneling of electrons to and from the silicon substrate at lower control gate voltages than is possible in the prior art.

Figures 4A-4I are useful in illustrating the methods of forming a novel memory cell, transistor or floating gate transistor according to the teachings of the present invention. According to the teachings of the present invention an edge-defined poly-silicon vertical gate is defined over the thin gate oxide in the active device area. This vertical gate is re-oxidized and another poly-silicon layer is deposited over the structure, and anisotropically or directionally etched to define another polysilicon vertical gate. These can be either symmetrical gate structures as shown and described in connection with Figure 2A or asymmetrical gate structures as shown and described in connection with Figure 3A. The methods of the present invention result in a novel memory cell which has a larger capacitance between the control gate and the floating gate, and only a smaller capacitance between the floating gate and the substrate. Thus, according to the teachings of the present invention, smaller control gate voltages than are required by conventional memory devices will result in large potential differences between the floating gate and substrate. This is due to the fact that the capacitance ratio as illustrated in Figures 2B, 2C, 3B, and 3C is more advantageous in the novel memory cell embodiments of the present invention.

Figure 4A illustrates the structure after the first sequence of processing steps. In Figure 4A, a thin gate oxide 401 is formed over an active device area 404, between a pair of field isolation oxides (FOXs) 420, in a horizontal surface of a substrate 400. The thin gate oxide 401 is formed to a first oxide thickness (t1). In one embodiment, the thin gate oxide 401 is formed to a thickness (t1) of approximately 60 Angstroms (Å). One of ordinary skill in the art will understand upon reading this disclosure the various suitable manners in which a thin gate oxide 401 can be formed over the active device area 403. For example, in one embodiment, the thin gate oxide can be formed by thermal oxidation, and the FOXs

can be formed using local oxidation of silicon (LOCOS) as the same are known and understood by one of ordinary skill in the art. After growth of the thin gate oxide 401 by thermal oxidation, and the LOCOS isolation 420, a thick layer of sacrificial oxide 402 is deposited over the surface of the thin gate oxide 401. In one embodiment, the thick layer of sacrificial oxide 402 is deposited to a thickness of approximately 0.5 micrometers (μm) using a low-pressure chemical vapor deposition (LPCVD) technique. Using a photoresist mask, according to photolithography techniques which are known and understood by one of ordinary skill in the art, this thick oxide 402 is etched. The desired thin-oxide 401 can be regrown in the areas not covered by the remaining thick sacrificial oxide 402. According to one embodiment of the present invention, an inductively coupled plasma reactor (ICP) using CHF_3 may be employed for this etching as the same is disclosed in an article by N.R. Rueger et al., entitled "Selective etching of SiO_2 over polycrystalline silicon using CHF_3 in an inductively couples plasma reactor", J. Vac. Sci. Technol., A, 17(5), p. 2492-2502, 1999. Alternatively, a magnetic neutral loop discharge plasma can be used to etch the thick oxide 402 as disclosed in an article by W. Chen et al., entitled "Very uniform and high aspect ratio anisotropy SiO_2 etching process in magnetic neutral loop discharge plasma", ibid, p. 2546-2550. The latter is known to increase the selectivity of SiO_2 to photoresist and/or silicon. The structure is now as appears in Figure 4A.

Figure 4B illustrates the structure following the next sequence of fabrication steps. In Figure 4B, a polysilicon layer 406 is deposited to a thickness of approximately 200 nanometers (nm). A conventional chemical vapor deposition (CVD) reactor may be used to deposit polycrystalline silicon films at substrate temperature in excess of 650° Celsius (C). In an alternative embodiment, a plasma-enhanced CVD process (PECVD) can be employed if a lower thermal budget is desired. In another alternative embodiment, a microwave-excited plasma enhanced CVD of poly-silicon using SiH_4/Xe at temperature as low as 300°C can be performed to deposit the polysilicon layer 406 as disclosed by Shindo et al., ibid. p.

3134-3138. According to this process embodiment, the resulting grain size of the polysilicon film was measured to be approximately 25 nm. Shindo et al. claim that the low-energy (approximately 3 eV), high-flux, ion bombardment utilizing Xe ions on a growing film surface activates the film surface and successfully enhances the surface reaction/migration of silicon, resulting in high quality film formation at low temperatures. In another alternative embodiment, the polysilicon layer 406 can be formed at an even lower temperature, e.g. 150° C, with and without charged species in an electron cyclotron resonance (ECR) plasma-enhanced CVD reactor as disclosed in an article by R. Nozawa et al., entitled "Low temperature polycrystalline silicon film formation with and without charged species in an electron cyclotron resonance SiH_4 plasma-enhanced chemical vapor deposition", ibid, p. 2542-2545. In this article, R. Nozawa et al. describe that in using an atomic force microscope they found that the films formed without charged species were smoother than those films formed with charged species. According to the teachings of the present invention, it is important to keep the smoothness of polysilicon layer 406. This will be evident from reading the subsequently described process steps in which another polysilicon layer will be fabricated later onto polysilicon layer 406 with a very thin insulation layer between them. The structure is now as appears in Figure 4B.

Figure 4C illustrates the structure following the next sequence of processing steps. Figure 4C shows a cross section of the resulting vertical gate structures, 407A and 407B, over the active device area 404 after the polysilicon layer 406 has been anisotropically etched. As shown in Figure 4C, the polysilicon vertical gate structures, 407A and 407B, remain only at the sidewalls of the thick sacrificial oxide 402. In one embodiment, the polysilicon layer 406 is anisotropically etched such that the vertical gate structures, 407A and 407B remaining at the sidewalls of the thick sacrificial oxide 402 have a horizontal width (W1) of approximately 100 nanometers (nm). In one embodiment, the polysilicon layer 406 can be anisotropically etched to form the vertical gate structures, 407A and 407B, through

the use of a high-density plasma helicon source for anisotropic etching of a dual-layer stack of poly-silicon on Si_{1-x} Ge_x as described in an article by Vallon et al., entitled "Poly-silicon-germanium gate patterning studies in a high density plasma helicon source", J. Vac. Sci. technol., A, 15(4), p. 1874-80, 1997. The same is incorporated herein by reference. In this article, wafers were described as being etched in a low pressure, high density plasma helicon source using various gas mixtures of Cl_2, HBr, and O_2. Also, according to this article, process conditions were optimized to minimize the gate oxide 401 consumption. The structure is now as shown in Figure 4C.

Figure 4D illustrates the structure after the next series of process steps. In Figure 4D, the thick sacrificial oxide 402 is removed. As one of ordinary skill in the art will understand upon reading this disclosure the thick sacrificial oxide layer can be removed using any suitable, oxide selective etching technique. As shown in Figure 4D, the remaining polysilicon vertical gate structures, 407A and 407B, are oxidized to form insulator, intergate dielectric, oxide layer, or silicon dioxide (SiO_2) layer 409. In one embodiment, a conventional thermal oxidation of silicon may be utilized at a high temperature, e.g. greater than 900° C. In an alternative embodiment, for purposes of maintaining a low thermal budget for advanced ULSI technology, a lower temperature process can be used. One such low temperature process includes the formation of high-quality silicon dioxide films by electron cyclotron resonance (ECR) plasma oxidation at temperature as low as 400° C as described in an article by Landheer, D. et al., entitled "Formation of high-quality silicon dioxide films by electron cyclotron resonance plasma oxidation and plasma-enhanced chemical vapor deposition", Thin Solid Films, vol. 293, no. 1-2, p. 52-62, 1997. The same is incorporated herein by reference. Another such low temperature process includes a low temperature oxidation method using a hollow cathode enhanced plasma oxidation system as described in an article by Usami, K. et al., entitled "Thin Si oxide films for MIS tunnel emitter by hollow cathode enhanced plasma oxidation", Thin Solid Films, vol. 281-282, no. 1-2, p. 412-414, 1996. The

same is incorporated herein by reference. Yet another low temperature process includes a low temperature VUV enhanced growth of thin silicon dioxide films at low temperatures below 400° C as described in an article by Patel, P. et al., entitled "Low temperature VUV enhanced growth of thin silicon dioxide films", Applied Surface Science, vol. 46, p. 352-6, 1990. The same is incorporated herein by reference.

Figure 4E shows the structure following the next series of steps. In Figure 4E, another, or second, polysilicon layer 411 is formed over the oxide layer 409 to a thickness of approximately 100 nm. Forming the second polysilicon layer 411 over the oxide layer 409 can be performed using any similar technique to those used in forming the first polysilicon layer 406 as described in detail in connection with Figure 4B. As shown in Figure 4E, the second polysilicon layer 411 will be separated by a second oxide thickness, or second insulator thickness (t2) from the active device region 404 which is slightly greater than the thin tunnel oxide thickness, e.g. first oxide thickness or first insulator thickness (t1) which separates the vertical gate structures 407A and 407B from the substrate 400. In one embodiment the second oxide thickness, or second insulator material thickness (t2) is approximately 100 Angstroms (Å) thick. The structure is now as appears in Figure 4E.

Figure 4F illustrates the structure after the next series of steps. In Figure 4F, the structure is once again subjected to an anisotropic etch. The anisotropic etch includes the anisotropic etching process used for etching the first polysilicon layer 406 to form the vertical gate structures 407A and 407B as described in more detail in connection with Figure 4C. Figure 4F shows one embodiment of the present invention in which the resulting structure is symmetrical, including two groups of three free standing vertical polysilicon gates. The two groups of three free standing vertical gates include the original vertical gate structures 407A and 407B, and new vertical gate structures 413A and 413B parallel to and on opposing sides of each

original vertical gate structures 407A and 407B. This structure embodiment is now as appears in Figure 4F.

In Figure 4G, the process is continued to form horizontal polysilicon gate structures above the original vertical gate structures 407A and 407B, and new vertical gate structures 413A and 413B on opposing sides of each original vertical gate structures 407A and 407B. In Figure 4G, the new vertical gate structures 413A and 413B are connected by forming a third polysilicon layer 415 over a top surface of the structure shown in Figure 4F. The third polysilicon layer 415 can be formed over the top surface of the structure shown in Figure 4F using any similar technique to those used in forming the first polysilicon layer 406 as described in detail in connection with Figure 4B. In one embodiment, according to the teachings of the present invention, the third polysilicon layer 415 is formed to a thickness of approximately 100 nm. In one embodiment, forming the third polysilicon layer 415 is followed by masking and etching techniques, as the same have been described above, in order to leave horizontal polysilicon gate structures 415 only above and connecting the vertical gate structures 413A and 413B. The structure is now as appears in Figure 4G. Figure 4G thus represent a symmetrical structure embodiment of the present invention in which the vertical gate structures 413A and 413B, which are parallel to and on opposing sides of each vertical gate structures 407A and 407B, are coupled by the horizontal polysilicon gate structures 415 above the vertical gate structures 407A and 407B. As shown in Figure 4G, the vertical gate structures 413A and 413B coupled by the horizontal polysilicon gate structures 415 are isolated from vertical gate structures 407A and 407B by insulator layer or oxide layer 409.

In one embodiment, illustrated by Figure 4H, the structure of Figure 4G can be anisotropically etched using masking techniques known to one of ordinary skill in the art, as well as the anisotropic etching processes described in connection with Figure 4F, to produce asymmetrical vertical gate structures. These asymmetrical vertical gate structures will include the original vertical gate structures 407A and

407B, and one remaining vertical gate structure, either 413A or 413B on one side or the other of each original vertical gate structures 407A and 407B as well as a horizontal gate structure 415 depending on the chosen condition of the anisotropic etch process. That is, the anisotropic etch can be performed to leave horizontal gate structure 415 coupled to and above either vertical gate structure 413A or 413B on one side or the other of each original vertical gate structures 407A and 407B. The same is shown in Figure 4H.

The next series of process steps can continue from either Figures 4G or 4H. For purposes of illustration, Figure 4I provides an illustration of the process steps continued from Figure 4G. However, one of ordinary skill in the art will understand that analogous process steps may be used to continue the fabrication process from the structure shown in Figure 4H. In Figure 4I, the structure from Figure 4G is oxidized to form an oxide layer of approximately 50 nm. The oxidation process of the structure shown in Figure 4G can be performed using any suitable technique as the same has been describe above. An ion implantation is then performed to activate source regions shown as 410A and 410B as well as drain region 412. In Figure 4I, the drain region 412 is illustrated as shared between vertical gate structure 407A and 407B.

One of ordinary skill in the art will understand that other source and drain region configurations can be activated through various ion implantation techniques. Additionally, in one embodiment, the source and/or drain regions can be fabricated with source and/or drain extensions, e.g. similar to source extensions shown in connection with Figure 3A for facilitating tunneling, by using a masking step and another implantation as the same is known and understood by one of ordinary skill in the art of memory technology. Further conventional process steps can then be used to contact the source, drain and control gate portions of the structure to complete the device of either Figure 2A or Figure 3A.

As described above, the structures can be completed such that vertical gates 407A and 407B serve as floating gates for the device structures and vertical gates

413A and 413B serve as control gates. Alternatively, the structures can be completed such that vertical gates 407A and 407B serve as a control gate for the device structures and vertical gates 413A and 413B serve as floating gates.

As will be understood by reading this disclosure, the memory cells, or floating gate transistors, of the present invention can be fabricated such that the total capacitance of the device is about the same as that of prior art horizontal or vertical floating gate transistor structures, e.g. Figures 1A and 1B, of comparable source/drain spacings. However, now since the floating gate capacitance (CFG) for the novel memory cells of the present invention is much smaller than the control gate capacitance (CCG) the majority of any voltage applied to the control gate will appear across the floating gate thin tunnel oxide 401. The floating gate can then be programmed and erased by tunneling of electrons to and from the source of the transistor at relatively low voltages, or programmed by hot electron injection and erased by tunneling.

The operation of the novel memory cells of the present invention is illustrated in connection with Figure 5A-5E. As explained above, the novel device of the present invention will function on tunneling of electrons to and from the source region of the device for both writing and erase operations, or operate in a tunnel-tunnel mode in conjunction with hot electron injection.

Figure 5A-5B illustrate the operation of the novel memory cell of Figure 2A when the outer vertical gates serve as the control gate. In this embodiment, the novel device 501 of the present invention will function on tunneling of electrons to and from the channel region 506 of the device 501 for both writing and erase operations as the same are known and understood by one of ordinary skill in the art. As shown in Figure 5A, if no electrons are stored on the floating gate 507, then when a potential is applied to the control gate 513, the region of the channel 511-1 beneath the floating gate 507 will actually have a slightly lower threshold voltage (Vt) than the other regions of the channel where the slightly thicker gate oxides (t2) separate the control gate 513 from the channel 506, and the transistor will readily

turn on, at lower than conventional control gate voltages, when a read voltage is applied to the control gate 513. In this respect the device functions in a manner analogous to a flash memory cell. On the other hand, as shown in Figure 5B, if electrons are stored on the floating gate 507, this region of the channel 511-1 beneath the floating gate 507 will have a high threshold voltage (Vt) and will not turn on and conduct when the same low voltage is applied to the control gate 513 to read the memory cell. There are simply no electrons in this region of the channel 511-1 beneath the floating gate 507 to conduct.

An alternative embodiment is to interchange the functions of the gates, the inner gate 507 becoming the control gate 507 and the outer gate 513 becoming the floating gate 513 as shown in Figures 5C-5D. In this embodiment, as shown in Figure 5C, again with no electrons stored on the floating gate 513, when a potential is applied to the control gate 507, the region of the channel beneath 511-1 the control gate 507 will actually have a slightly lower threshold voltage (Vt) than the other regions of the channel where the slightly thicker gate oxides (t2) separate the floating gate 513 from the channel 506, and the transistor will readily turn on at lower than conventional control gate 507 voltages, when a read voltage is applied to the control gate 507. On the other hand, as shown in Figure 5D, if electrons are stored on the floating gate 513, the other regions of the channel where the slightly thicker gate oxides (t2) separate the floating gate 513 from the channel 506 will have a high threshold voltage (Vt) and will not turn on and conduct when the same low voltage is applied to the control gate 507 to read the memory cell. There are simply no electrons in these other regions of the channel, e.g. regions 511-2 and 511-3 where the slightly thicker gate oxides (t2) separate the floating gate 513 from the channel 506, to conduct.

As shown in Figure 5E, in this later embodiment of Figures 5C-5D, the erase operation will be performed using source side 510 tunneling. The write operation, however, will use hot electron injection from the channel region 506 at the drain region 512 to write electrons on to the floating gate 513 as is commonly done in

some flash memory cells. As one of ordinary skill will understand upon reading this disclosure, similar operation modes can be employed based on the particular floating gate to control gate configuration selection for the structure embodiment shown in Figure 3A.

Figure 6 is a schematic drawing illustrating one circuit diagram embodiment and application of the novel memory cell shown in Figure 2A in a NOR type memory cell with two devices 601A and 601B. In the embodiment shown in Figure 6, the two devices 601A and 601B share a common drain 612. As explained in detail above, according to the teachings of the present invention, vertical gates 602A and 602B are included. Further the two devices 601A and 601B include vertical gates 604A and 604B. These vertical gates, 602A, 602B, 604A and 604B, are formed over horizontal body regions, 608A and 608B respectively, in devices 601A and 601B. The horizontal body regions will conduct between source regions 606A and 606B, respectively, and the common drain region 612 according to the conditions detailed and described above for the novel memory cells of the present invention. As one of ordinary skill in the art will understand upon reading this disclosure, the NOR circuit embodiment of Figure 6 can similarly substitute the novel memory cell structure shown in Figure 3A for the two devices 601A and 601B. The invention is not so limited. Further, as one of ordinary skill in the art will understand upon reading this disclosure, other circuit diagram embodiments can similarly be configured using the novel memory cells of the present invention. As one of ordinary skill in the art will understand upon reading this disclosure, these devices can be used in a variety of flash memory, EEPROM, and/or EAPROM arrays and applications. The invention is not so limited.

Figure 7 illustrates a block diagram of an embodiment of an electronic system 701 according to the teachings of the present invention. In the embodiment shown in Figure 7, the system 701 includes a memory device 700 which has an array of memory cells 702, address decoder 704, row access circuitry 706, column access circuitry 708, control circuitry 710, and input/output circuit 712. Also, as

shown in Figure 7, the circuit 701 includes a processor 714, or memory controller for memory accessing. The memory device 700 receives control signals from the processor 714, such as WE*, RAS* and CAS* signals over wiring or metallization lines. The memory device 700 is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 700 has been simplified to help focus on the invention. At least one of the memory cells 702 has a memory cell formed according to the embodiments of the present invention.

It will be understood that the embodiment shown in Figure 7 illustrates an embodiment for electronic system circuitry in which the novel memory cells of the present invention. The illustration of system 701, as shown in Figure 7, is intended to provide a general understanding of one application for the structure and circuitry of the present invention, and is not intended to serve as a complete description of all the elements and features of an electronic system using the novel memory cell structures. Further, the invention is equally applicable to any size and type of memory device 701 using the novel memory cells of the present invention and is not intended to be limited to the described above. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

Applications containing the novel memory cell of the present invention as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

Figure 8 illustrates an embodiment of a memory array 800, according to the teachings of the present invention, as can be included in a memory device, e.g. on a

memory chip/die. The memory array shown in Figure 8 includes a plurality of memory cells, 802-0, 802-1, . . ., 802-N. The plurality of memory cells, 802-0, 802-1, . . ., 802-N, includes at least one novel memory cell formed according to the teachings of the present invention. As shown in Figure 8, the plurality of memory cells are coupled to a plurality, or number of sense amplifiers 806-0, 806-1, . . ., 806-N via a number of bit lines, or digitlines, D0*, D0, D1*, D1, . . ., DN*. Figure 8 is illustrative of the manner in which the novel memory cell of the present invention can be used in a folded bit line configuration, in substitution for a conventional folded bit line memory array. One of ordinary skill in the art will understand upon reading this disclosure, that the novel memory cells of the present invention can further be used in an open bit line configuration or any other digitline twist scheme. The invention is not so limited.

The Figures presented and described in detail above are similarly useful in describing the method embodiments of operation for novel memory cell of the present invention. That is one embodiment of the present invention includes applying a first potential across a thin tunneling oxide between a vertical floating gate and a first portion of a horizontal substrate in order to add or remove a charge from the floating gate. As described in detail above, the horizontal substrate includes a source region and a drain region separated by a horizontal channel region. This method embodiment further includes reading the memory cell by applying a second potential to a vertical control gate located above a second portion of the horizontal substrate. The vertical control gate is parallel to and opposing the vertical floating gate.

Another method embodiment of the present invention includes writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate. This method embodiment includes erasing a charge from a vertical floating gate to a source region in a horizontal substrate by applying a second potential to the vertical control gate. This method embodiment further includes reading the memory cell by applying a third potential to the vertical

control gate. Applying a first, second, and third potential to the vertical control gate includes applying a first, second, and third potential to a vertical control gate which is parallel to and opposing the vertical floating gate. In one embodiment for one of the novel memory cell structures described above, the method of writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate includes tunneling electrons from a horizontal channel in the horizontal substrate to the vertical floating gate using Fowler Nordheim tunneling. In another embodiment for another of the novel memory cell structures described above, the method of writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate includes using a hot electron injection technique to tunnel electrons at a drain region in the horizontal substrate to the vertical floating gate. Erasing a charge from a vertical floating gate to a source region in a horizontal substrate by applying a second potential to the vertical control gate includes tunneling electrons from the vertical floating gate to the source region in a horizontal substrate using Fowler Nordheim tunneling.

Another method embodiment of the present invention includes using a vertical control gate to add and remove a charge to a vertical floating gate. This method embodiment includes using the charge stored on the vertical floating gate to modulate a horizontal conduction channel beneath the vertical floating gate. The method further includes sensing a conduction level through the horizontal channel to sense a state of the memory cell. According to the teachings of the present invention, the conduction level through the horizontal channel is modulated by a charge level in a vertical floating gate.

Another method embodiment of the present invention includes storing a charge in a vertical floating gate and using the charge stored in the vertical floating gate to control a threshold voltage level required to create conduction in a horizontal channel region beneath the vertical floating gate.

CONCLUSION

Thus, the present invention provides structures and methods for memory devices which operate with lower control gate voltages than conventional flash, EEPROM, and/or EAPROM devices. The structures and methods of the present invention use thin silicon dioxide (SiO_2) layers as an insulator material, in place of higher dielectric constant materials, for separating the control gate and floating gate. Thus, the structures and methods of the present invention do not increase the costs or complexity of the device fabrication process. These systems and methods are fully scalable with shrinking design rules and feature sizes in order to provide even higher density integrated circuits. The total capacitance of these memory devices is about the same as that for the prior art floating gate transistor devices of comparable source and drain spacings. However, according to the teachings of the present invention, the floating gate capacitance is much smaller than the control gate capacitance such that the majority of any voltage applied to the control gate will appear across the floating gate thin tunnel oxide allowing the device to operate with lower control gate voltages. In sum, the devices of the present invention can be programmed by tunneling of electrons to and from the silicon substrate at lower control gate voltages than is possible in the prior art.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A memory cell, comprising:

a source region in a horizontal substrate;

a drain region in the horizontal substrate;

a channel region separating the source and the drain regions;

a vertical floating gate located above a portion of the channel region and separated from the channel region by a first thickness insulator material; and

at least one vertical control gate located above another portion of the channel region and separated therefrom by a second thickness insulator material, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate, and wherein the at least one vertical control gate is separated from the vertical floating gate by an intergate dielectric.

2. The memory cell of claim 1, wherein the at least one vertical control gate has a horizontal width of approximately 100 nanometers (nm).

3. The memory cell of claim 1, wherein the first thickness insulator material is approximately 60 Angstroms (Å), and wherein the second thickness insulator material is approximately 100 Angstroms (Å).

4. The memory cell of claim 1, wherein the first thickness insulator material, the second thickness insulator material, and the intergate dielectric include silicon dioxide (SiO_2).

5. The memory cell of claim 1, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 Angstroms (Å).

6. The memory cell of claim 1, wherein the intergate dielectric has a thickness approximately equal to the first thickness insulator material.

7. A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a vertical floating gate separated from a first portion of the channel region by a first oxide thickness; and

at least one vertical control gate separated from a second portion of the channel region by a second oxide thickness, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate.

8. The transistor of claim 7, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 nanometers (nm).

9. The transistor of claim 7, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

10. The transistor of claim 7, wherein the at least one vertical control gate has a horizontal width of approximately 100 Angstroms (Å).

11. The transistor of claim 7, wherein the vertical floating gate separated from a first portion of the channel region includes a first portion of the channel region which is adjacent to the source region, and wherein the at least one vertical control gate separated from a second portion of the channel region includes a second portion of the channel region which is adjacent to the drain region.

12. The transistor of claim 11, wherein the at least one vertical control gate further includes a horizontal member located above the vertical floating gate, wherein the at least one vertical control gate an the horizontal member are separated from the vertical floating gate by an intergate dielectric.

13. The transistor of claim 7, wherein a capacitance between the at least one vertical control gate and the floating gate is greater than a capacitance between the floating gate and the channel.

14. A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness; and

a third vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness.

15. The floating gate transistor of claim 14, wherein the second and the third vertical gates are parallel to and on opposing sides of the first vertical gate.

16. The floating gate transistor of claim 14, wherein the first vertical gate includes a floating gate and wherein the second and the third vertical gates include control gates.

17. The floating gate transistor of claim 14, wherein first vertical gate includes a control gate and wherein the second and the third vertical gates include floating gates.

18. The floating gate transistor of claim 14, wherein the floating gate transistor further includes a horizontal gate member which couples the second and the third vertical gates.

19. The floating gate transistor of claim 14, wherein a greater percentage of a voltage applied to the second and the third vertical gates appears between the first vertical gate and the channel than between the first vertical gate and the second and the third vertical gates.

20. The floating gate transistor of claim 14, wherein the second and the third portion of the channel region are adjacent the source region and the drain region, respectively.

21. The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

22. The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate each have a horizontal width of approximately 100 nanometers (nm).

23. The floating gate transistor of claim 14, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

24. A memory device, comprising:

a plurality of memory cells, wherein each memory cell includes:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first vertical gate separated from a first portion of the channel region by a first oxide thickness; and

a second vertical gate separated from a second portion of the channel region by a second oxide thickness, wherein the second vertical gate is parallel to and opposing the first vertical gate; and

at least one sense amplifier, wherein the at least one sense amplifier couples to the plurality of memory cells.

25. The memory device of claim 24, wherein each memory cell includes a flash memory cell.

26. The memory device of claim 24, wherein each memory cell includes an electronically eraseable and programmable read only memory (EEPROM) cell.

27. The memory device of claim 24, wherein the first vertical gate includes a floating gate and the second vertical gate includes a control gate.

28. The memory device of claim 24, wherein the first vertical gate includes a control gate and the second vertical gate includes a floating gate.

29. The memory device of claim 24, wherein the first vertical gate and the second vertical gate have a horizontal width of approximately 100 nanometers (nm).

30. The memory device of claim 24, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

31. The memory device of claim 24, wherein the first vertical gate separated from a first portion of the channel region by a first oxide thickness includes a first portion of the channel region which is adjacent to the source region.

32. The memory device of claim 24, wherein the second vertical gate separated from a second portion of the channel region by a second oxide thickness includes a second portion of the channel region which is adjacent to the source region.

33. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes a plurality of memory cells coupled to at least one sense amplifier, and wherein each memory cell includes:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first vertical gate separated from a first portion of the channel region by a first oxide thickness; and

a second vertical gate separated from a second portion of the channel region by a second oxide thickness, wherein the second vertical gate is parallel to and opposing the first vertical gate.

34. The electronic system of claim 33, wherein each memory cell includes a flash memory cell.

35. The electronic system of claim 34, wherein each memory cell further includes a third vertical gate separated from a third portion of the channel region by the second oxide thickness, and wherein the second and the third vertical gates are parallel to and on opposing sides of the first vertical gate.

36. The electronic system of claim 35, wherein the first vertical gate, the second vertical gate, and the third vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

37. The electronic system of claim 34, wherein the first vertical gate includes a floating gate and the second vertical gate includes a control gate.

38. The electronic system of claim 34, wherein the first vertical gate includes a control gate and the second vertical gate includes a floating gate.

39. The electronic system of claim 34, wherein the first vertical gate and the second vertical gate have a horizontal width of approximately 100 nanometers (nm).

40. The electronic system of claim 34, wherein the first oxide thickness is approximately equal to an intergate dielectric thickness which separates the first vertical gate and the second vertical gate.

41. The electronic system of claim 34, wherein the second vertical gate separated from a second portion of the channel region by a second oxide thickness includes a second portion of the channel region which is adjacent to the source region.

42. The electronic system of claim 34, wherein the first vertical gate further includes a horizontal member located above the second vertical gate.

43. The electronic system of claim 34, wherein a capacitance between the first vertical gate and the second vertical gate is greater than a capacitance between either the first vertical gate or the second vertical gate and the channel.

44. A method for forming a memory cell, comprising:

forming a source region and a drain region separated by a channel region in a horizontal substrate;

forming a first vertical gate above a first portion of the channel region and separated from the channel region by a first oxide thickness (t1); and

forming a second vertical gate above a second portion of the channel region and separated from the channel region by a second oxide thickness (t2), wherein forming the second vertical gate includes forming the second vertical gate parallel to and opposing the first vertical gate.

45. The method of claim 44, wherein the method further includes forming a flash memory cell.

46. The method of claim 44, wherein forming the first vertical gate includes forming a floating gate, and wherein forming the second vertical gate includes forming a control gate.

47. The method of claim 44, wherein forming the first vertical gate and forming the second vertical gate include forming the first and the second vertical gates to have a horizontal width of approximately 100 nanometers (nm).

48. The method of claim 44, wherein forming a first vertical gate separated from the channel region by a first oxide thickness (t1) includes forming the first vertical gate separated from the channel region by a first oxide thickness (t1) of approximately 60 Angstroms (Å).

49. The method of claim 44, wherein forming a second vertical gate separated from the channel region by a second oxide thickness (t2) includes forming the second vertical gate separated from the channel region by a second oxide thickness (t2) of approximately 100 Angstroms (Å).

50. The method of claim 44, wherein forming the first vertical gate separated from a first portion of the channel region by a first oxide thickness (t1) includes forming the first vertical gate separated from a first portion of the channel region which is adjacent to the source region.

51. The method of claim 44, wherein forming the second vertical gate separated from a second portion of the channel region by a second oxide thickness includes forming the second vertical gate separated from a second portion of the channel region which is adjacent to the source region.

52. A method for forming a floating gate transistor, comprising:

forming a source region and a drain region separated by a channel region in a horizontal substrate;

forming a first vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

forming a second vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness; and

forming a third vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness.

53. The method of claim 52, wherein forming the second and the third vertical gates includes forming the second and the third vertical gates parallel to and on opposing sides of the first vertical gate.

54. The method of claim 52, wherein forming the first vertical gate includes forming a floating gate and wherein forming the second and the third vertical gates includes forming control gates.

55. The method of claim 52, wherein forming the first vertical gate includes forming a control gate and wherein forming the second and the third vertical gates includes forming floating gates.

56. The method of claim 52, wherein forming the floating gate transistor further includes forming a horizontal gate member which couples the second and the third vertical gates.

57. The method of claim 52, wherein forming the second and the third vertical gates over a second and a third portion of the channel region, respectively, includes forming the second and the third vertical gates adjacent to the source region and the drain region, respectively.

58. The method of claim 52, wherein forming the first, the second, and the third vertical gates includes forming polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

59. The method of claim 52, wherein forming the first, the second, and the third vertical gates includes forming each gate to have a horizontal width of approximately 100 nanometers (nm).

60. The method of claim 52, wherein forming a first vertical gate separated from the channel region by a first oxide thickness includes forming a first oxide thickness of approximately 60 Angstroms (Å), and wherein forming a second vertical gate

separated from the channel region by a second oxide thickness includes forming a second oxide thickness of approximately 100 Angstroms (Å).

61. A method for operating a memory cell, comprising:

applying a first potential across a thin tunneling oxide between a vertical floating gate and a first portion of a horizontal substrate, the horizontal substrate including a source region and a drain region separated by a horizontal channel region, in order to add or remove a charge from the floating gate; and

reading the memory cell by applying a second potential to a vertical control gate located above a second portion of the horizontal substrate, wherein the vertical control gate is parallel to and opposing the vertical floating gate.

62. A method for operating a memory cell, comprising:

writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate;

erasing a charge from a vertical floating gate to a source region in a horizontal substrate by applying a second potential to the vertical control gate; and

reading the memory cell by applying a third potential to the vertical control gate.

63. The method of claim 62, wherein applying a first, second, and third potential to the vertical control gate includes applying a first, second, and third potential to a vertical control gate which is parallel to and opposing the vertical floating gate.

64. The method of claim 62, wherein writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate includes tunneling electrons from a horizontal channel in the horizontal substrate to the vertical floating gate using Fowler Nordheim tunneling.

65. The method of claim 62, wherein writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate includes using a hot electron injection technique to tunnel electrons at a drain region in the horizontal substrate to the vertical floating gate.

66. The method of claim 62, wherein erasing a charge from a vertical floating gate to a source region in a horizontal substrate by applying a second potential to the vertical control gate includes tunneling electrons from the vertical floating gate to the source region in a horizontal substrate using Fowler Nordheim tunneling.

67. A method for operating a memory cell, comprising:

using a vertical control gate to add and remove a charge to a vertical floating gate; and

using the charge stored on the vertical floating gate to modulate a horizontal conduction channel beneath the vertical floating gate.

68. The method of claim 67, wherein method further includes sensing a conduction level through the horizontal channel to sense a state of the memory cell, wherein the conduction level is modulated by a charge level in a vertical floating gate.

69. A method for operating a memory cell, comprising:

storing a charge in a vertical floating gate; and

using the charge stored in the vertical floating gate to control a threshold voltage level to create conduction in a horizontal channel region beneath the vertical floating gate.

HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES

Abstract of the Disclosure

Structures and methods for memory devices are provided which operate with lower control gate voltages than conventional floating gate transistors, and which do not increase the costs or complexity of the device fabrication process. In one embodiment of the present invention, the novel memory cell includes a source region and a drain region separated by a channel region in a horizontal substrate. A first vertical gate is separated from a first portion of the channel region by a first oxide thickness. A second vertical gate is separated from a second portion of the channel region by a second oxide thickness. According to the teachings of the present invention, the total capacitance of these memory devices is about the same as that for the prior art of comparable source and drain spacings. However, according to the teachings of the present invention, the floating gate capacitance (CFG) is much smaller than the control gate capacitance (CCG) such that the majority of any voltage applied to the control gate will appear across the floating gate thin tunnel oxide.

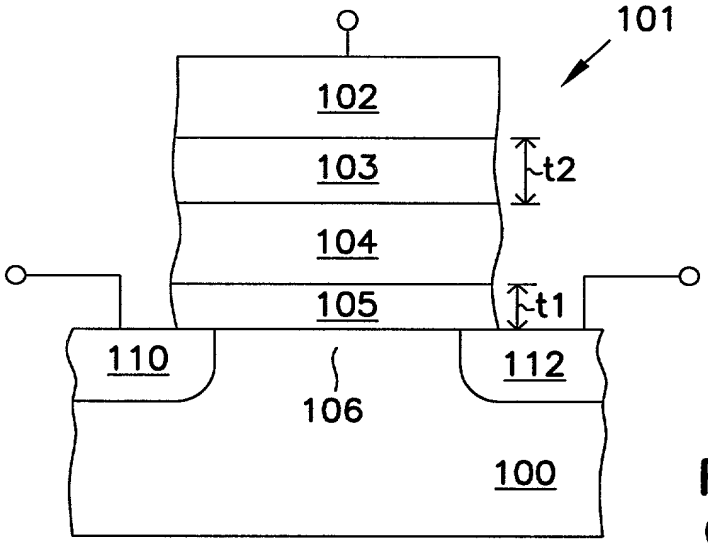

FIG. 1A
(Prior Art)

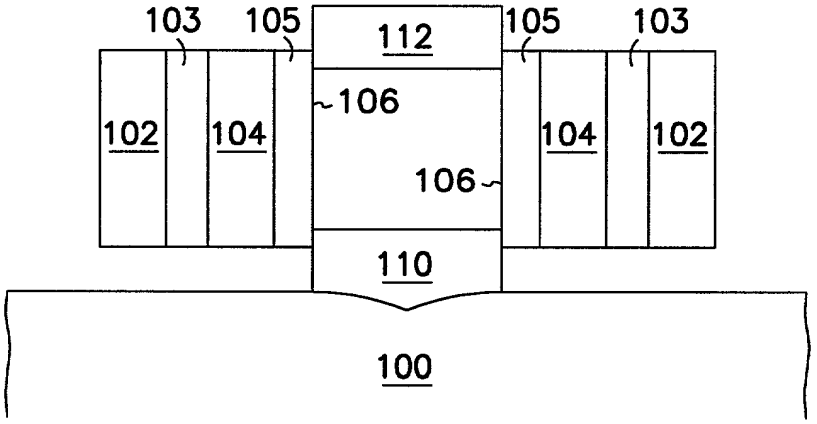

FIG. 1B
(Prior Art)

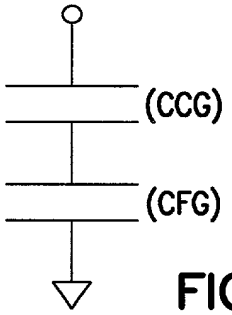

FIG. 1C
(Prior Art)

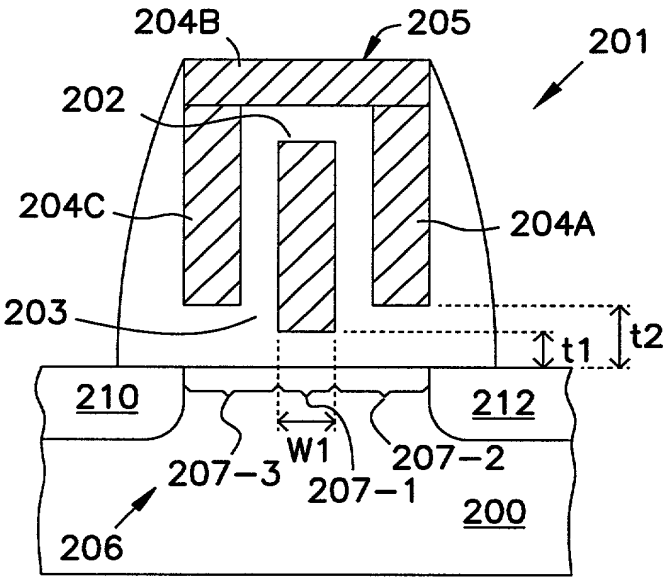

FIG. 2A

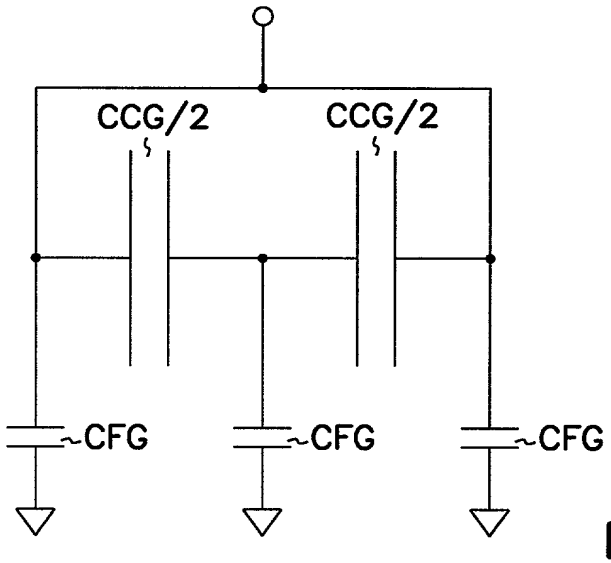

FIG. 2B

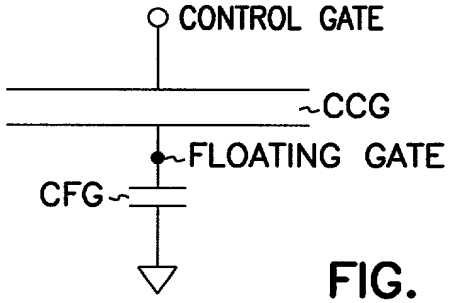

FIG. 2C

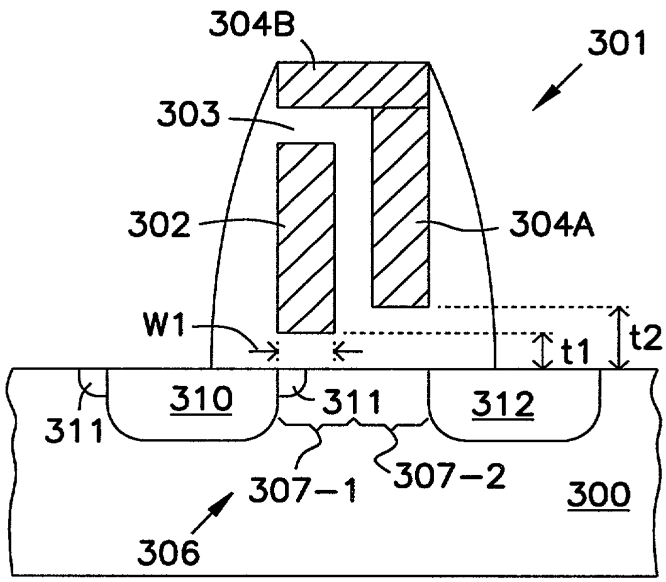

FIG. 3A

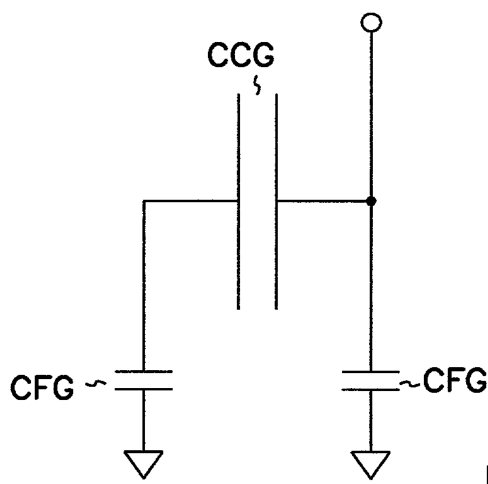

FIG. 3B

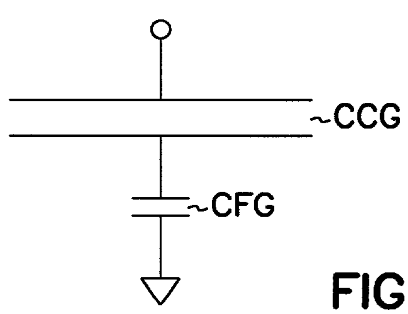

FIG. 3C

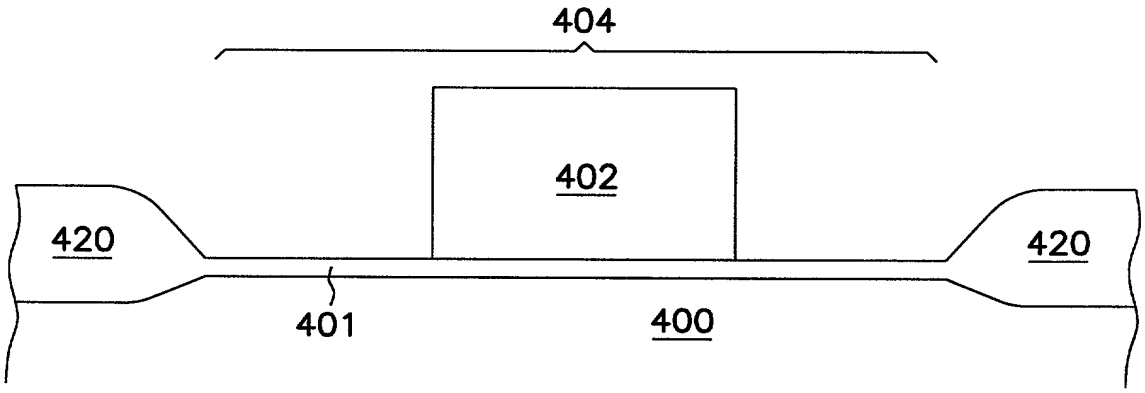

FIG. 4A

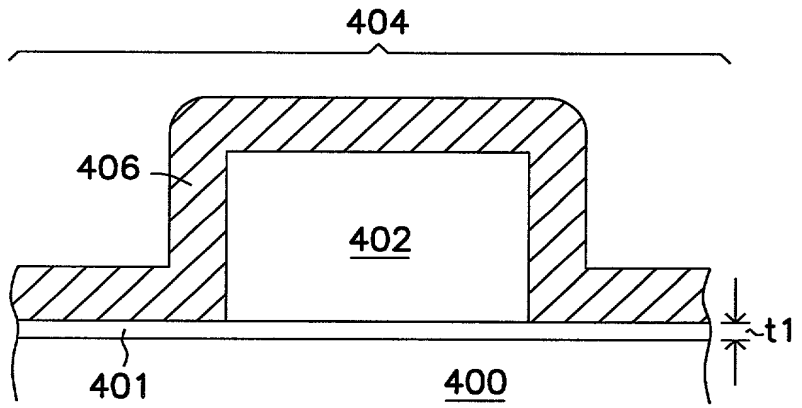

FIG. 4B

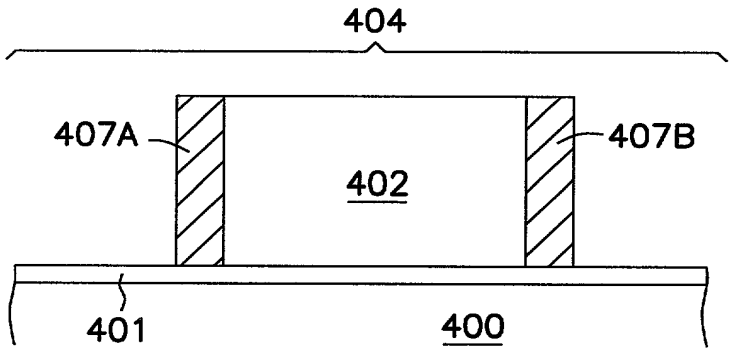

FIG. 4C

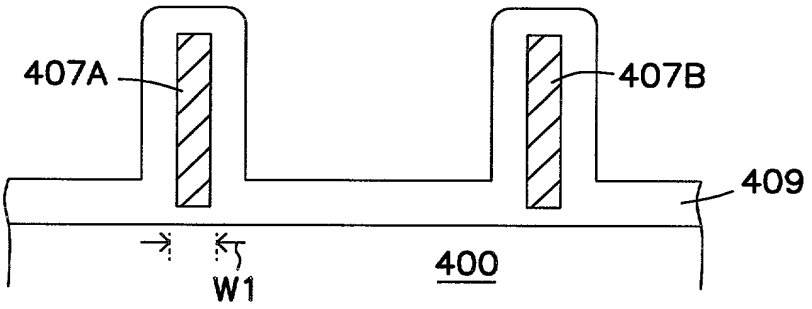

FIG. 4D

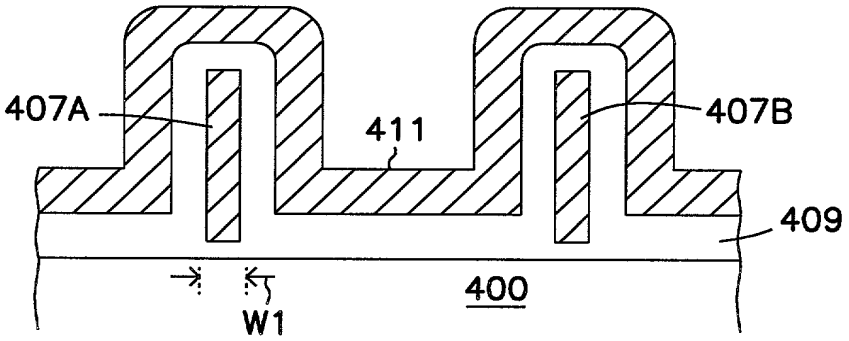

FIG. 4E

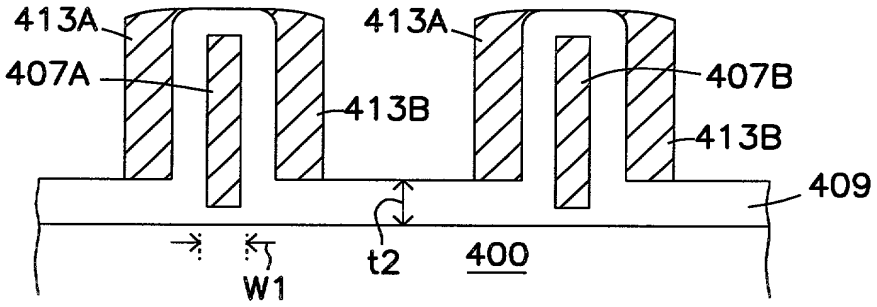

FIG. 4F

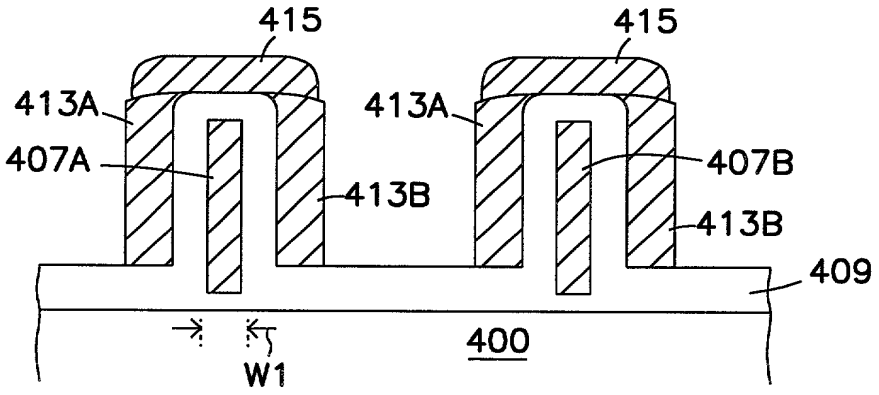

FIG. 4G

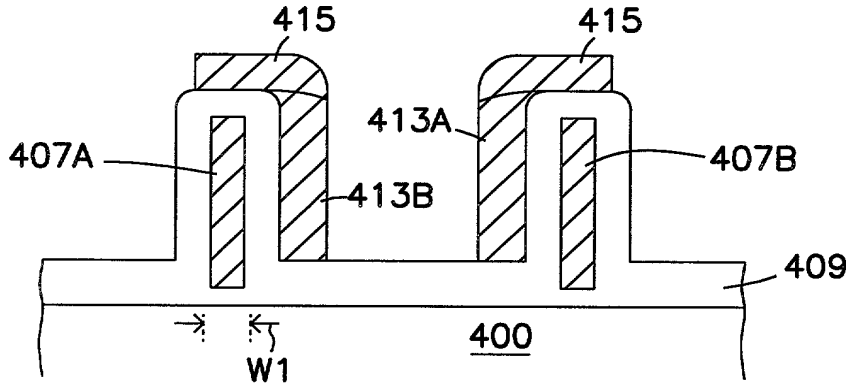

FIG. 4H

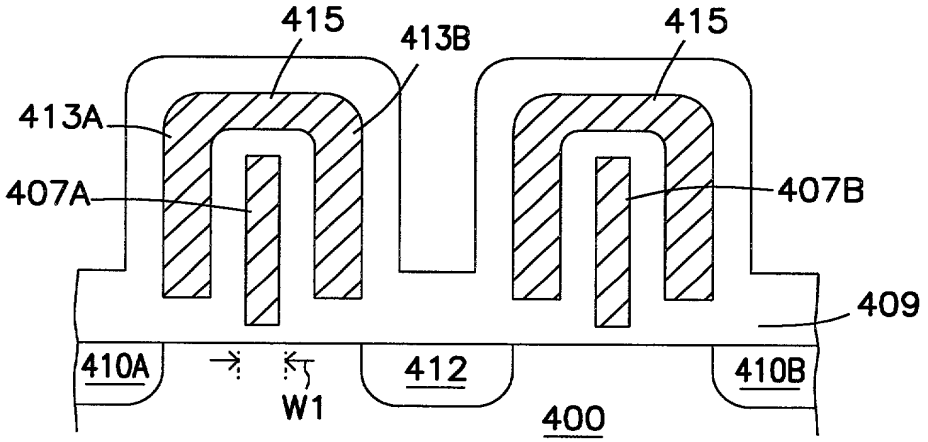

FIG. 4I

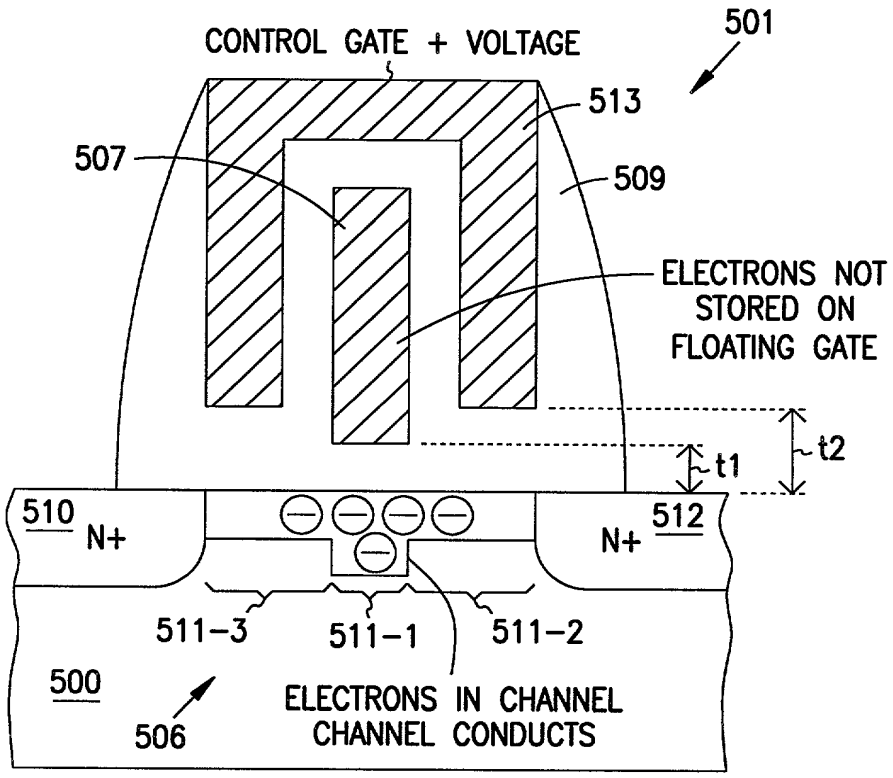
CONTROL GATE + VOLTAGE
501
513
507
509
ELECTRONS NOT
STORED ON
FLOATING GATE
t1
t2
510
N+
512
N+
511-3
511-1
511-2
500
506
ELECTRONS IN CHANNEL
CHANNEL CONDUCTS

FIG. 5A

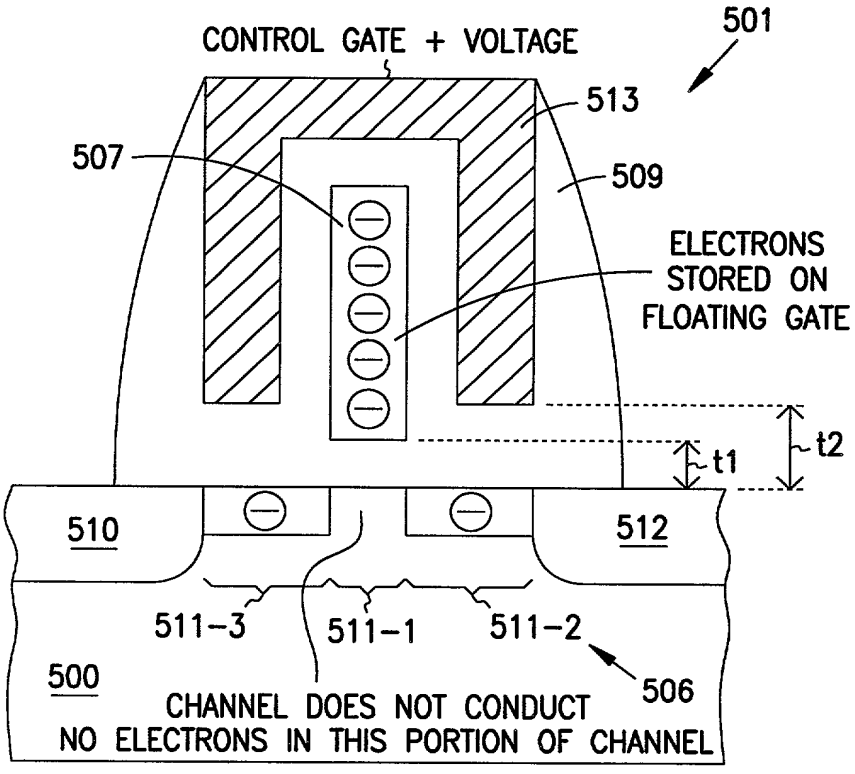
CONTROL GATE + VOLTAGE
501
513
507
509
ELECTRONS
STORED ON
FLOATING GATE
t1
t2
510
512
511-3
511-1
511-2
500
506
CHANNEL DOES NOT CONDUCT
NO ELECTRONS IN THIS PORTION OF CHANNEL

FIG. 5B

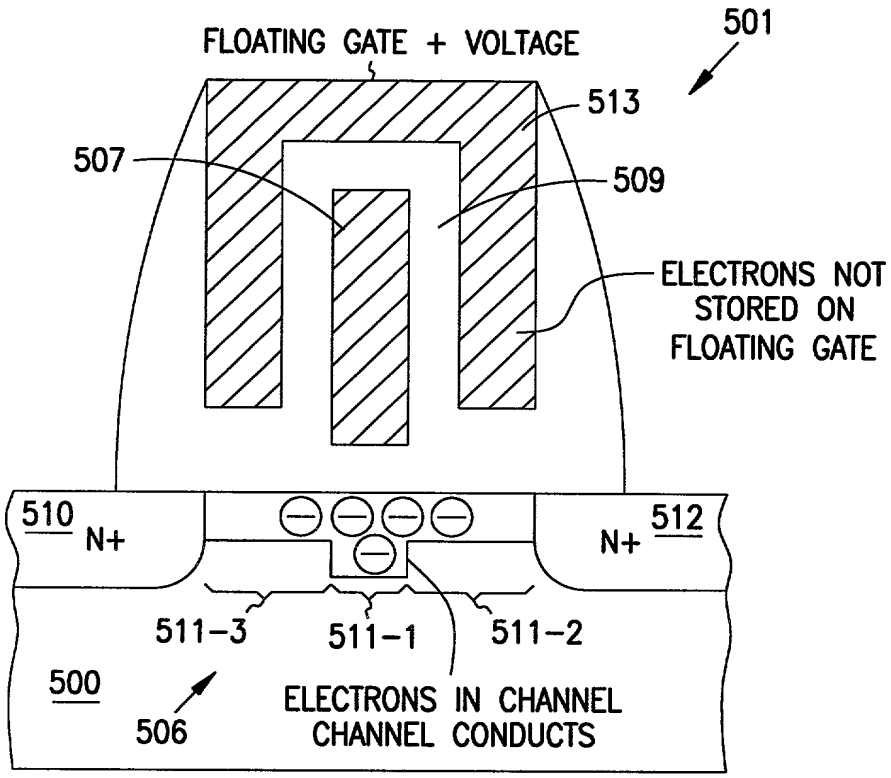
FLOATING GATE + VOLTAGE
501
513
507
509
ELECTRONS NOT
STORED ON
FLOATING GATE
510
N+
512
N+
511-3
511-1
511-2
500
506
ELECTRONS IN CHANNEL
CHANNEL CONDUCTS

FIG. 5C

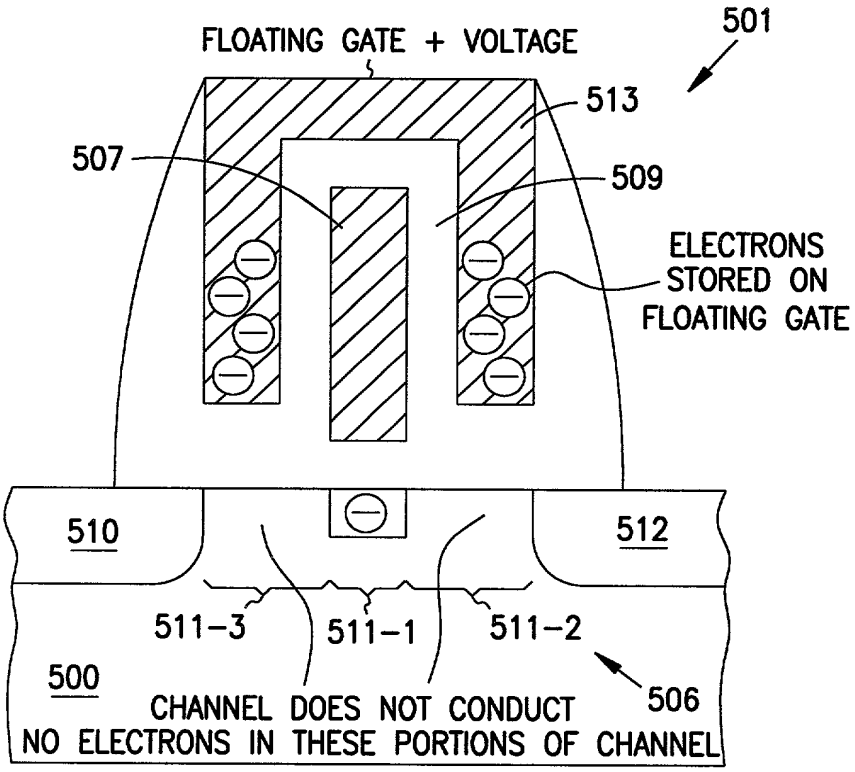
FLOATING GATE + VOLTAGE
501
513
507
509
ELECTRONS
STORED ON
FLOATING GATE
510
512
511-3
511-1
511-2
500
506
CHANNEL DOES NOT CONDUCT
NO ELECTRONS IN THESE PORTIONS OF CHANNEL

FIG. 5D

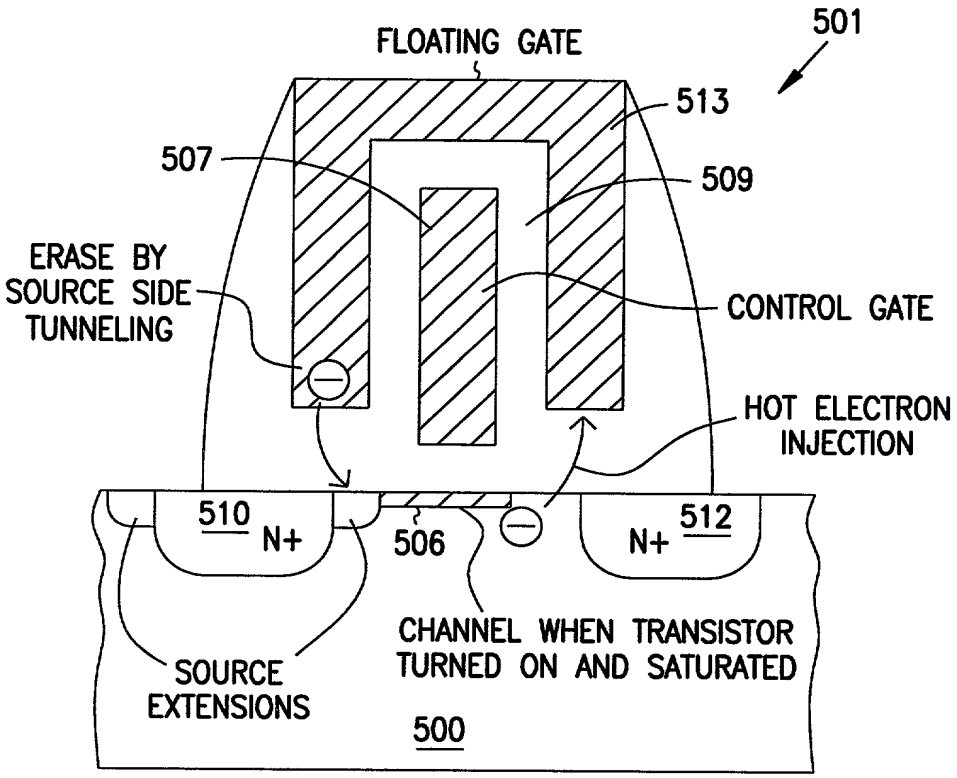
501
FLOATING GATE
513
507
509
ERASE BY
SOURCE SIDE
TUNNELING
CONTROL GATE
HOT ELECTRON
INJECTION
510
N+
506
N+
512
CHANNEL WHEN TRANSISTOR
TURNED ON AND SATURATED
SOURCE
EXTENSIONS
500

FIG. 5E

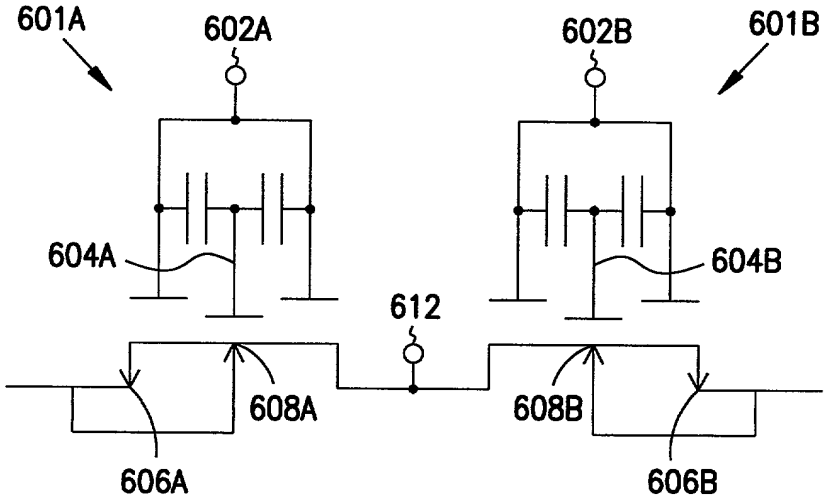
601A
602A
602B
601B
604A
604B
612
608A
608B
606A
606B

FIG. 6

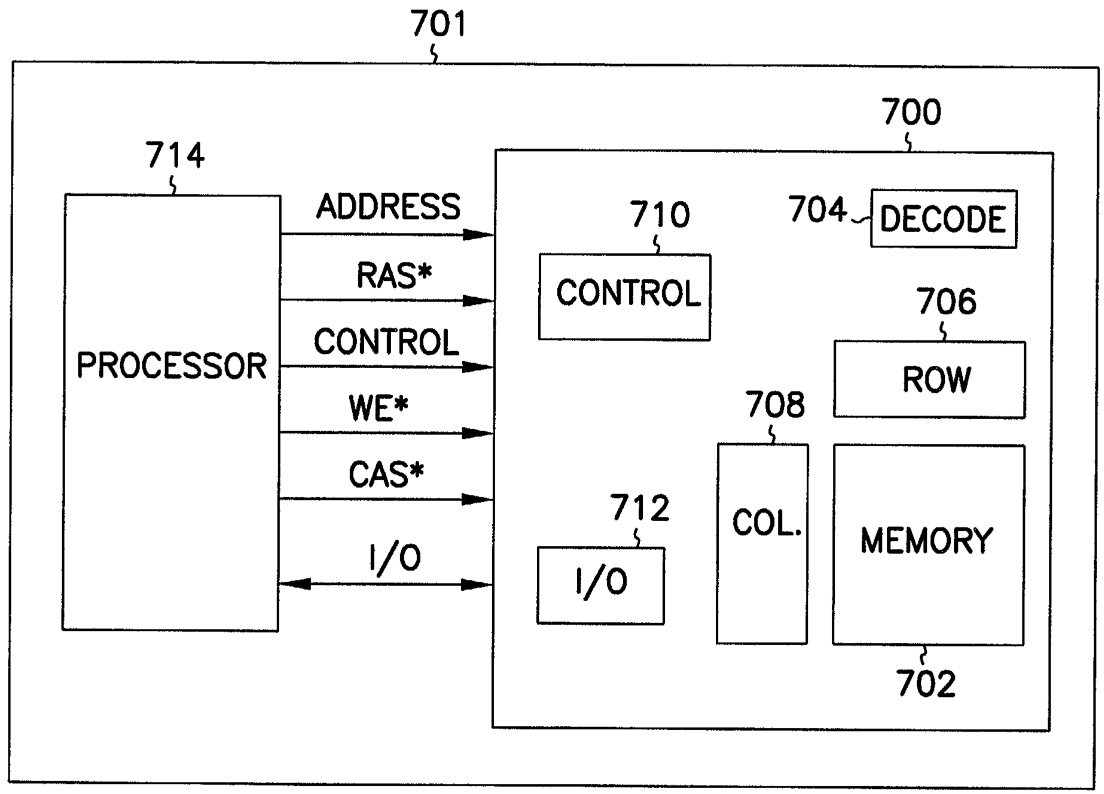

FIG. 7

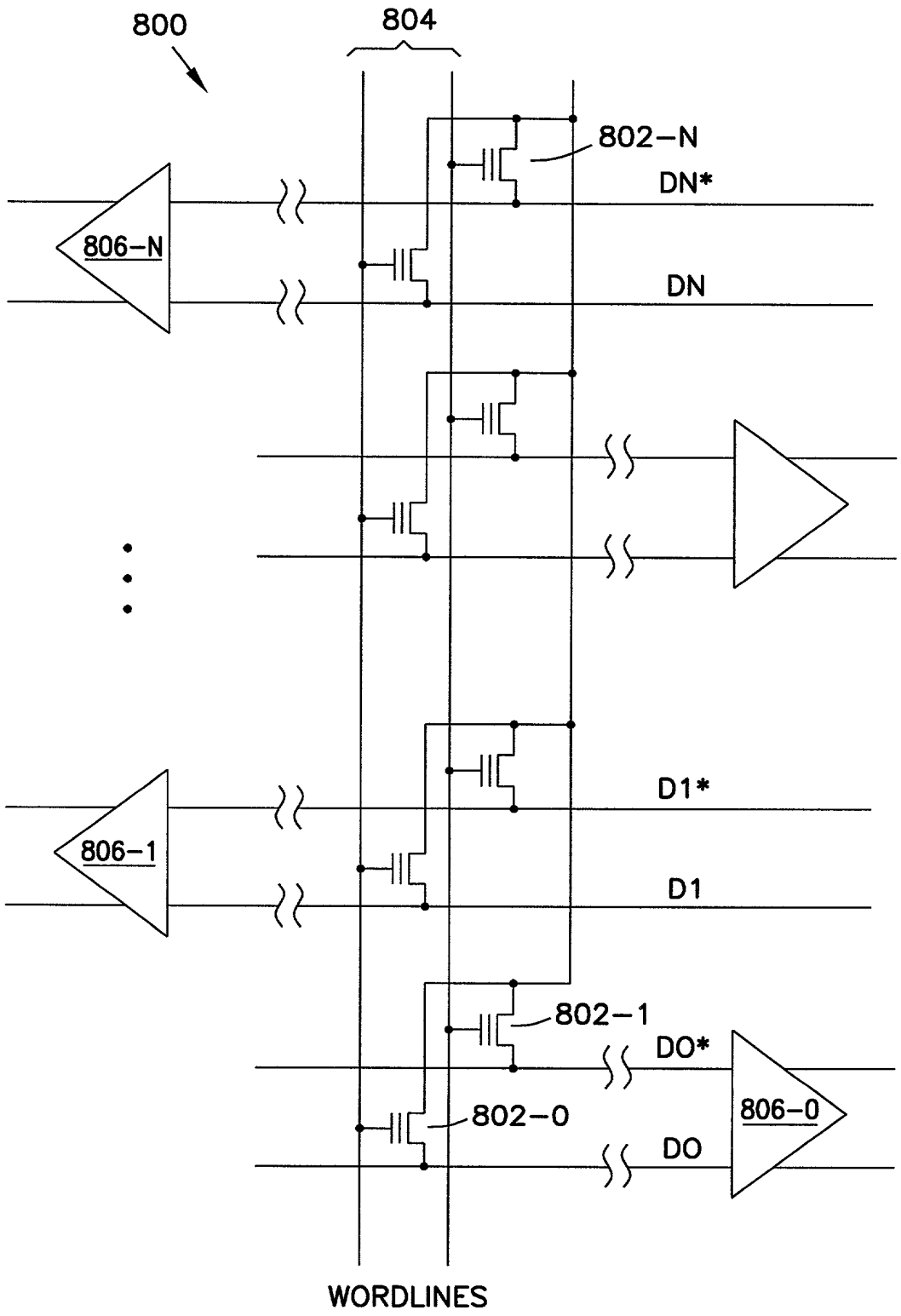
800
804
802-N
DN*
806-N
DN
D1*
806-1
D1
802-1
DO*
802-0
806-0
DO
WORDLINES

FIG. 8

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: 29 APR 2000
~~Leonard~~ Forbes

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: April 27, 2000
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.691US1	
Title:	HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Anglin, J. Michael	Reg. No. 24,916	Jurkovich, Patti J.	Reg. No. 44,813	Nelson, Albin J.	Reg. No. 28,650
Bianchi, Timothy E.	Reg. No. 39,610	Kalis, Janal M.	Reg. No. 37,650	Nielsen, Walter W.	Reg. No. 25,539
Billion, Richard E.	Reg. No. 32,836	Kaufmann, John D.	Reg. No. 24,017	Oh, Allen J.	Reg. No. 42,047
Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Padys, Danny J.	Reg. No. 35,635
Brennan, Leoniede M.	Reg. No. 35,832	Kluth, Daniel J.	Reg. No. 32,146	Parker, J. Kevin	Reg. No. 33,024
Brennan, Thomas F.	Reg. No. 35,075	Lacy, Rodney L.	Reg. No. 41,136	Perdok, Monique M.	Reg. No. 42,989
Brooks, Edward J., III	Reg. No. 40,925	Leffert, Thomas W.	Reg. No. 40,697	Prout, William F.	Reg. No. 33,995
Chu-Dinh C.P.	Reg. No. 41,676	Lemaire, Charles A.	Reg. No. 36,198	Schumm, Sherry W.	Reg. No. 39,422
Clark, Barbara J.	Reg. No. 38,107	Litman, Mark A.	Reg. No. 26,390	Schwegman, Micheal L.	Reg. No. 25,816
Dahl, John M.	Reg. No. 44,639	Lundberg, Steven W.	Reg. No. 30,568	Smith, Michael G.	Reg. No. 45,368
Drake, Eduardo E.	Reg. No. 40,594	Mack, Lisa K.	Reg. No. 42,825	Speier, Gary J.	Reg. No. 45,458
Eliseeva, Maria M.	Reg. No. 43,328	Maeyaert, Paul L.	Reg. No. 40,076	Steffey, Charles E.	Reg. No. 25,179
Embretson, Janet E.	Reg. No. 39,665	Maki, Peter C.	Reg. No. 42,832	Terry, Kathleen R.	Reg. No. 31,884
Fordenbacher, Paul J.	Reg. No. 42,546	Malen, Peter L.	Reg. No. 44,894	Tong, Viet V.	Reg. No. 45,416
Forrest, Bradley A.	Reg. No. 30,837	Mates, Robert E.	Reg. No. 35,271	Viksnins, Ann S.	Reg. No. 37,748
Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. 42,858	Woessner, Warren D.	Reg. No. 30,440
Huebsch, Joseph C.	Reg. No. 42,673	Nama, Kash	Reg. No. 44,255		

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: Edward J. Brooks, III
P.O. Box 2938
Minneapolis, MN 55402

Telephone: (612) 373-6913
Facsimile: (612) 339-3061

Dated: 5-16-00

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel